Who Watches the Watcher?
Detecting Hypervisor Introspection from Unprivileged Guests
Overview

“The Cloud”

• Numerous organizations are moving en masse to the cloud
  – It’s easier to manage
  – It’s easier to scale
• This results in a loss of control of physical hardware and privileges on the system
  – Everything is tied to guest virtual machines
Overview

Hypervisors (Virtual Machine Monitors)

• The root-of-trust is the hypervisor (virtual machine monitor)
  - It can introspect on guests with **few restrictions**
  - It can introspect on guests with **little evidence of apparent action**
Overview

Hypervisors (Virtual Machine Monitors)

• This trade-off puts organizations and individuals in a difficult situation
  - They have **sensitive data and processes**
  - Compromises are **expensive and dangerous**
Overview

Related Work

• Compromise of or introspection by a hypervisor has been a known issue

• Previous work on hypervisor detection has focused on hardware or software artifacts
  - This is more oriented towards detection of past events rather active introspection
Motivation

- A hypervisor’s activities are **not entirely invisible** to its guests
- **System performance is impacted** as the hypervisor seeks to provide an environment which is functionally equivalent to native hardware
- Increases in an instruction’s **execution time and/or cache artifacting** can provide evidence of a hypervisor’s intervention
Implementation

- A **test framework** emulates inappropriate introspection.

- A **monitoring module** on the guest employs a set of sensors to detect malicious behavior.
Test Framework

• The Xen Project was used as the hypervisor
• Modifications were made to support hypercalls which would toggle introspection capabilities
• Modifications were made to support instructions that Xen Project does not support VM-exiting for
Monitoring Module and Sensors

- **Instruction intercession sensors** detect intercession of instruction execution using intercession timing.
- **Active memory intercession sensors** detect the hypervisor actively interceding in memory access operations.
- **Passive memory monitoring sensors** detect when a hypervisor accesses memory externally to a guest.
- **Non-temporal access sensors** are not completed, but could be used to detect hypervisor introspection via non-caching page mappings or non-temporal instructions.
Background

Hypervisor

- Privileged software that handles **execution** and **isolation** of guest virtual machines.
Background

Virtual Machine Exits (VM-Exits)

- A hypervisor must be able to intercede in guest execution as necessary
- Guest execution is **paused** and execution is **handed to the hypervisor**
- Guest state information is stored in the Virtual Machine Control Structure (VMCS)
  - Resides in memory
  - Exits require that **state information is saved off during transition**
  - As such, an exit incurs significant overhead
Background

Timers & Timing Methods

• Time Stamp Counter (TSC)
• High Precision Event Timer (HPET)
• Thread racing
Background

LibVMI

• C and Python library that enables introspection on virtual machines
Background

Cache
Background

Cache

SET ASSOCIATIVE CACHE

4-WAY

4 SETS

CACHE LINE

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Instruction Intercession Sensors

• A hypervisor can trap on certain instructions to:
  • **Modify** the guest’s execution behavior
  • Determine when a guest **performs** various operations
  • **Extraction** of information
• Timing can be used to determine that this is happening, and how much work the hypervisor performed while trapping
Instruction Intercession Sensors

- Wall timing via the HPET
  - Manipulation of the HPET would result in noticeable interruptions in operations to the observer
- Thread racing
  - Parallel threads run, one of which executes NOPs, with number of executions counted upon completion
Active Memory Intercession Sensors

- Virtual to physical memory mappings can be marked to cause a VM-exit (using LibVMI)

- VM-exit incurs a sizable overhead, and resultant large timing increase
Passive Memory Monitoring Sensors

• A more stealthy hypervisor can choose to map the guest’s physical pages into other contexts
• Time required to access a memory line can be used
• Using Flush+Reload:
  • The memory line of interest is flushed from the cache
  • A period of time passes to allow for potential access to the memory region to occur
  • The memory line is reloaded, and the access is timed
• An decrease in timing is indicative of introspection
Non-Temporal Access Experimentation

- Non-temporal, streaming, and vector instructions have cache-coherence side-effects, despite bypassing the cache
  - A non-temporal instruction reading/writing a populated page triggers a cache flush
- Intel’s Page Attribute Table (PAT) allows specifying per-page caching behavior
  - Passive mappings can become non-cache-interacting
Analysis & Classification of Results

• A variety of machines are used which had different processor generations

• For instruction intercession, a baseline is derived from non-exiting instructions
  • Adequately high values can be flagged as potentially exiting, or of interest

• For memory intercession, baselines are observable from adjacent non-introspected memory
Results

Instruction Intercession

• Trapping by the hypervisor immediately returns, thus delivering the minimal possible impact on timing
Results

Instruction Intercession – Wall Timing

Wall Timing Results

[Graph showing wall timing results for various instructions]
Results

Instruction Interceision – Instruction Timing
Results

Instruction Interceッション – Wall Timing

![Wall Timing Results](chart.png)
Results

Instruction Interceッション – Instruction Timing

Instruction Timing Results

- Instruction Cycles

Non-Exiting: Exiting

Who Watches the Watcher? Detecting Hypervisor Introspection from Unprivileged Guests
Results

Active Memory Intercession

Memory Timing Results

- Cycle Time
- Page Offset
Results

Passive Memory Interception

Cache Timing Results

<table>
<thead>
<tr>
<th>Memory Address Offset</th>
<th>Cycle Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>300</td>
</tr>
<tr>
<td>0x100</td>
<td>275</td>
</tr>
<tr>
<td>0x1000</td>
<td>250</td>
</tr>
<tr>
<td>0x40</td>
<td>200</td>
</tr>
<tr>
<td>0x80</td>
<td>150</td>
</tr>
</tbody>
</table>
Future Work

Next Steps

• This is a **first look** into hypervisor detection technology
• A **continuous detection environment** could be implemented
• Full **binary classification** could better categorize introspection
• A **response strategy** when introspection is discovered
Future Work

Technology on the Horizon

• New virtualization extensions limit detection via timing since they reduce overhead
  • Virtualization Exceptions (#VE)
  • VMFUNC
• Sub-page permissions permit memory protections at a 128-byte granularity
Conclusion

- Detection of instruction intercession is possible
- Active and passive memory monitoring is possible
  - Isolating a memory region to a specific process may be necessary
  - Active and passive monitoring used in conjunction could obfuscate results of timing techniques
- This work establishes the **limitations of hypervisor introspection detection**
Questions?

• We intend to open-source this work [whenever we get around to it]